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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/982,452	10/17/2001	Manjunath D. Haritsa	SUN-P5403	7441

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EXAMINER	
TAT, BINH C	

ART UNIT	PAPER NUMBER
2825	

DATE MAILED: 12/17/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/982,452	HARITSA ET AL.	
	Examiner	Art Unit	
	Binh C. Tat	2825	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE ____ MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *29 September 2003*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-77* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-77* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *17 October 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. §§ 119 and 120

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

13)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application) since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

a) ☐ The translation of the foreign language provisional application has been received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121 since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____.
4) ☐ Interview Summary (PTO-413) Paper No(s). _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

1. This is a response to the response filed on 09/29/03. The applicant argument regarding Haritsa, Manjunath are not persuasive; therefore, all the rejections based on Haritsa, Manjunath are retained and repeated for the following reasons.

Terminal Disclaimer

The terminal disclaimer filed on 09/29/03 disclaiming the terminal portion of any patent granted on this application which would extend beyond the expiration date of any patent granted on Application Number 09/982459 has been reviewed and is accepted. The terminal disclaimer has been recorded.

Claim Rejections - 35 USC § 103

2. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have

been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Rejection of Claims 1-77

4. Claims 1-77 are rejected under 35 U.S.C. 103(a) as being unpatentable over Camporese et al. ("Camporese"), U.S. Patent 6,205,571 and Graef, U.S. Patent 6,305,001. Camporese discloses a clock tree distribution network for distributing a clock signal across a chip involving clock skew analysis. Although Camporese suggests Applicants' limitations, Camporese does not disclose a specific system for implementing the method. Graef also discloses a clock tree distribution planning method and additionally discloses a system for implementing the method that is a typical system used in IC designs. Graef further states that the system disclosed represents "one of many suitable computer platforms for implementing the method." (col. 15, II. 47-50). Both Camporese and Graef disclose a method involving a clock distribution network.. However, Graef details the system that would be necessary to implement methods involving clock distribution networks in general. It therefore would have been obvious to one of ordinary skill in the art at the time of Applicants' invention to use the system of Graef, or some similar system configuration, to implement the Camporese method.

5. Pursuant to claims 1, 16, 31, and 43 which recites a Clock Data Model (Fig. 2 illustrates this limitation; also, col. 3, II. 48-50 discloses a clock-related electrical simulation model) for use with a method of determining clock insertion delays for a microprocessor design having grid-based clock distribution comprising,

partitioning the complete clock net into a global clock net (the first level wiring networks, e.g. Figure 2, #201; reference the Fig. 2 description at col. 4, II. 25-28) and a plurality of local clock nets (the second level of tree wires, e.g. Figure 2, #203; reference the Figure 2 description at col. 4, II. 28-31);

simulating each of the plurality of local clock nets to generate a load for each of the plurality of local clock nets on the global clock net: col. 12, II. 12-23 wherein the twig wiring represents the local clock nets; additionally, the Nsector electrical lists comprise the loading for the plurality of local clock nets;.

simulating the global clock net based in part on the simulated load of each of the plurality of local clock nets: col. 12, II. 12-23 wherein the twig wiring represents the local clock nets;

combining the plurality of simulations to form the complete clock net: col. 11, II. 33-50;

6. Pursuant to claims 2, 17, 32, and 44 wherein partitioning comprises breaking the complete clock net into equal sized parts according to rectangular grid coordinates: Figure 2 illustrates this limitation.

7. Pursuant to claim 3, 18, 33 and 45 wherein the method further comprises breaking at least one of the plurality of local clock nets down into at least one sub-local clock net: col. 4, II. 28-31 suggests the existence of sub-local clock nets depending on the embodiment.

8. Pursuant to claim 4, 19, 34, and 46 wherein the method further comprises simulating the at least one sub-local clock net prior to simulating the corresponding local clock net: Fig. 7, step 735; col. 9, II. 60-64.

9. Pursuant to claims 5, 20, 35, and 47 wherein at least two of the plurality of local clock nets are simulated in parallel: Creation of isolated net lists which represent local clock nets and

are treated in parallel for tuning or simulation purposes, col. 9, II. 8-27; see also col. 9, II. 61-67 which discloses parallel tuning or simulation.

10. Pursuant to claims 6, 21, 36, 48 wherein simulating the clock nets comprises extracting a layout of the local clock net and the conductors routed above and through the local clock net from a microprocessor network database: the creation of the electrical netlist suggests this limitation, col. 6, II. 10-65;

extracting component values of the elements of the local clock net from the microprocessor network database: col. 6, II. 48-65;

simulating the local clock net based on the layout and the component values: col. 6, II. 48-65;

extracting a load of the local clock net on the global clock net: col. 6, II. 48-65.

11. Pursuant to claims 7, 22, 37, and 49 wherein simulating the local clock net comprises assuming that the clock arrival times form the global clock net will be simultaneous at all points where the local clock net is connected to the global clock net: col. 9, II. 35-43.

12. Pursuant to claims 8, 23 38, and 50wherein simulating the global clock net comprises extracting the layout of the global clock net from a microprocessor network database: the creation of the electrical netlist, col. 6, II. 10-65, details the layout connections;

extracting component values of the elements of the global clock from the microprocessor network database: col. 6, II. 48-65;

inserting the simulated loads of the plurality of local clock nets: col. 6, II. 48-54; see also col. 7, II. 13-15;

simulating the global clock net based on the layout, the component values, and the simulated local clock net loads: col. 6, II. 48-65.

13. Pursuant to claims 9, 24, 39 and 51 which further comprises storing the plurality of simulations in the Clock Data Model: col. 11, II. 19-22, wherein the tuned netlist represents the CDM with stored simulations.

14. Pursuant to claims 10, 25, 40 and 52 which further comprises evaluating the complete clock net to determine whether the results converge: col. 9, II. 35-60, wherein the true point load response matrix is checked against the smoothed point load response matrix which has calculations of clock signal arrival times.

15. Pursuant to claims 11, 26, 41,and 53 wherein if the results do not converge, replacing the clock arrival times with those calculated for the simulated global clock net: col. 9, lines 4756; re-simulating one of the plurality of local clock nets to generate a load for the local and global clock net: col. 12, II. 12-23;

re-simulating the global clock net based on the simulated or re-simulated load of each of the plurality of local clock nets: col. 12, II. 12-13 wherein the twig wiring represents the local clock nets.

combining the simulations and re-simulations to form the complete net: col. 11, II. 33-50.

16. Pursuant to claims 12, 27 and 54 wherein re-simulating the local clock net comprises resimulating the local clock net based on the layout, the component values, and the calculated clock arrival times: col. 6, II. 48-65;

extracting a load of the at least one local clock net on the global clock net: col. 6, II. 48-65.

17. Pursuant to claims 13, 28, and 55 wherein the method comprises re-simulating at least a second of the plurality of local clock nets in parallel with the at least one local clock net:

18. Pursuant to claims 14, 29 and 56 wherein re-simulating the global clock net comprises inserting the simulated or re-simulated loads of the plurality of local clock nets (col. 6, II. 48-54; see also col. 7, II. 13-15); and

re-simulating the global clock net based on the layout, the component values, and the simulated or re-simulated local clock net loads: col. 6, II. 48-65.

19. Pursuant to claim 15, 30, 42 and 57, wherein the method further comprises storing the plurality of re-simulations in the Clock Data Model: col. 11, II. 19-22.

20. Pursuant to Claim 58, 63, 68 and 73 which recites a Clock Data Model (Fig. 2 illustrates this limitation; also, col. 3, II. 48-50 discloses a clock-related electrical simulation model) for use with a method of determining clock insertion delays for a microprocessor design having grid-based clock distribution comprising,

partitioning the complete clock net into a global clock net (the first level wiring networks, e.g. Figure 2, #201; reference the Fig. 2 description at col. 4, II. 25-28) and a plurality of local clock nets (the second level of tree wires, e.g. Figure 2, #203; reference the Figure 2 description at col. 4, II. 28-31);

simulating each of the plurality of local clock nets to generate a load for each of the plurality of local clock nets on the global clock net: col. 12, II. 12-23 wherein the twig wiring represents the local clock nets; additionally, the Nsector electrical lists comprise the loading for the plurality of local clock nets;.

simulating the global clock net based in part on the simulated load of each of the plurality of local clock nets: col. 12, II. 12-23 wherein the twig wiring represents the local clock nets;

combining the plurality of simulations to form the complete clock net: col. 11, II. 33-50;

analyzing the complete clock net to predict the clock skew for a given data transfer path: black ground and fig 2-5 col 4-6.

21. Pursuant to claim 59, 64, 69, and 74 wherein analyzing comprises: adjusting an insertion delay of the involved elements of the given data transfer path: black ground and fig 2-5 col 4-6; and re simulating at least one local clock net involved in the given data transfer; black ground and fig 2-5 col 4-6.

22. Pursuant to claim 60-62, 65-67, and 75-77 further comprising, when the at least one re-simulated local clock net is connected to at least one sub-local clock net, evaluating the clock arrival times to determine whether the sub-local clock net should be re-simulated: black ground and fig 2-5 col 4-6.

Remarks

Applicant's response and remarks filed on 09/29/03 have been carefully review. Applicant's arguments have been fully considered but they are not persuasive. Key argument and their response related to the claims are listed as below:

23. The prior art (Camporese et al. US 6205571) does teach "a grid-based clock distribution" (see fig1-6 col 4 lines 40-59).

24. The prior art (Camporese et al. US 6205571) does teach "a layout of the local clock net and the conductors routed above and through the local clock net" (see fig 2 and fig 7 col 6 lines 10-43 fig 2 show how to layout the local clock net).

Conclusion

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

25. A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

26. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Binh C. Tat whose telephone number is (703) 305-4855. The examiner can normally be reached on 7:30 - 4:00 (M-F).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mathew Smith can be reached on (703) 308-1323. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 305-3431 for regular communications and (703) 305-3431 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-1782.

BINH TAT
Art Unit 2825
December 15, 2003

VUTHE SIEK
PRIMARY EXAMINER